

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

Jean-Francois AUTECHAUD

Serial No.: To Be Assigned

Filed: April 26, 2000

For: MODULAR INTERCONNECTION  
ARCHITECTURE FOR AN EXPANDABLE  
MULTIPROCESSOR MACHINE, USING A  
MULTILEVEL BUS HIERARCHY AND THE  
SAME BUILDING BLOCK FOR ALL THE  
LEVELS

Examiner:

Group Art Unit:

Corres. To FR99/05266  
Filed April 26, 1999

McLean, Virginia

**PROPOSED DRAWING CORRECTIONS**

Hon. Commissioner of Patents and Trademarks  
Washington, D.C. 20231

Sir:

Applicant requests approval of the drawing corrections on Figs. 1-5 as shown in red on the attached sheets.

The proposed corrections only comprise translating the French terms into English and removing the headings "1/5" to "5/5" to conform the drawings to U.S. practice.

Respectfully submitted,

Miles &amp; Stockbridge P.C.

Date: April 26, 2000

By:

  
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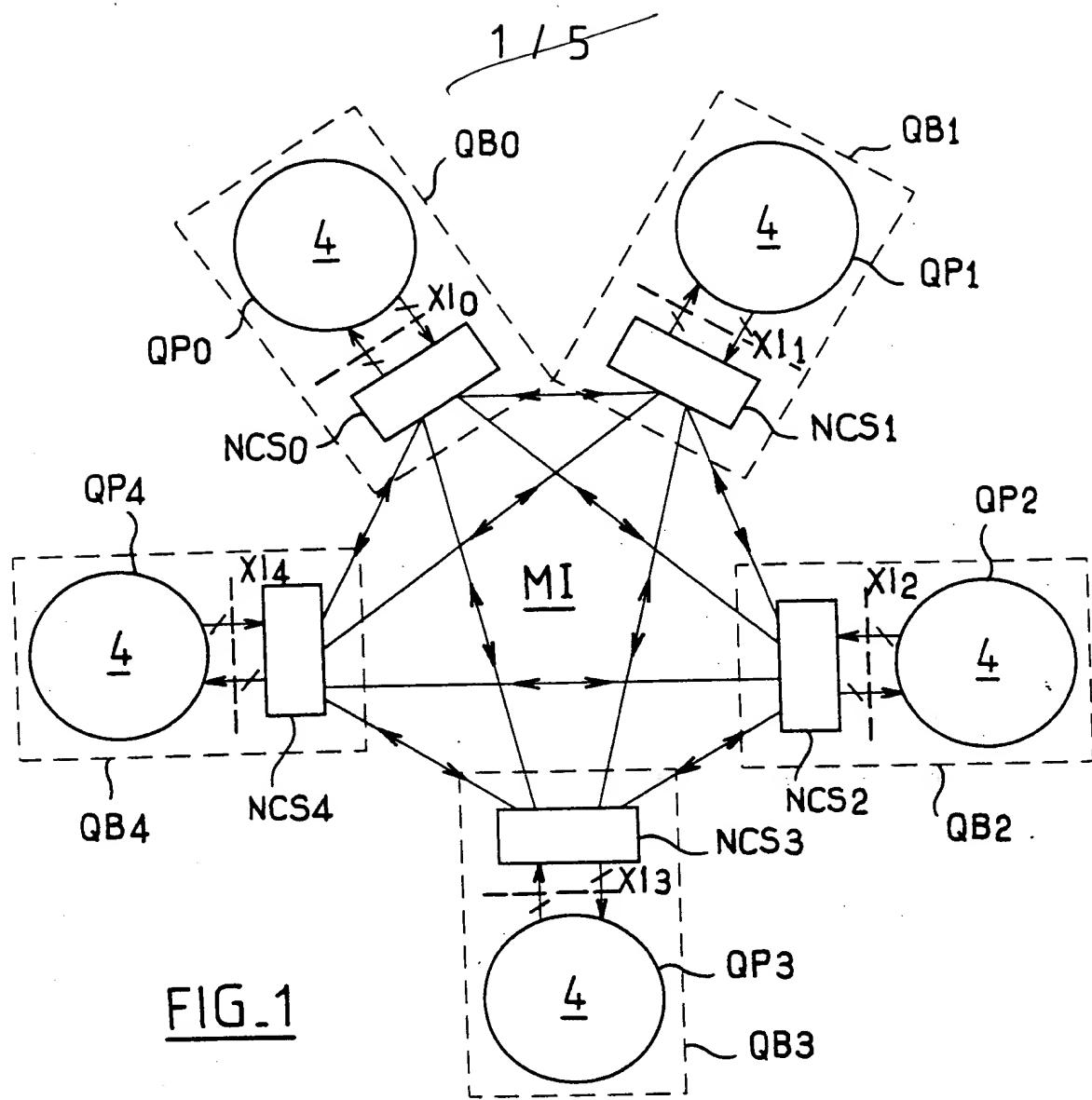


FIG.1

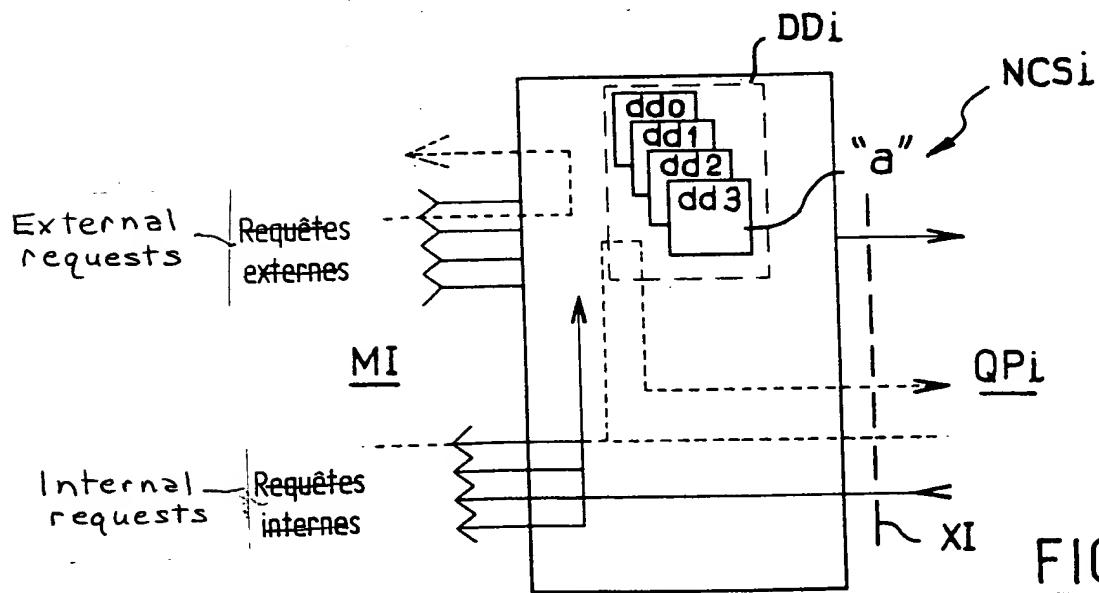
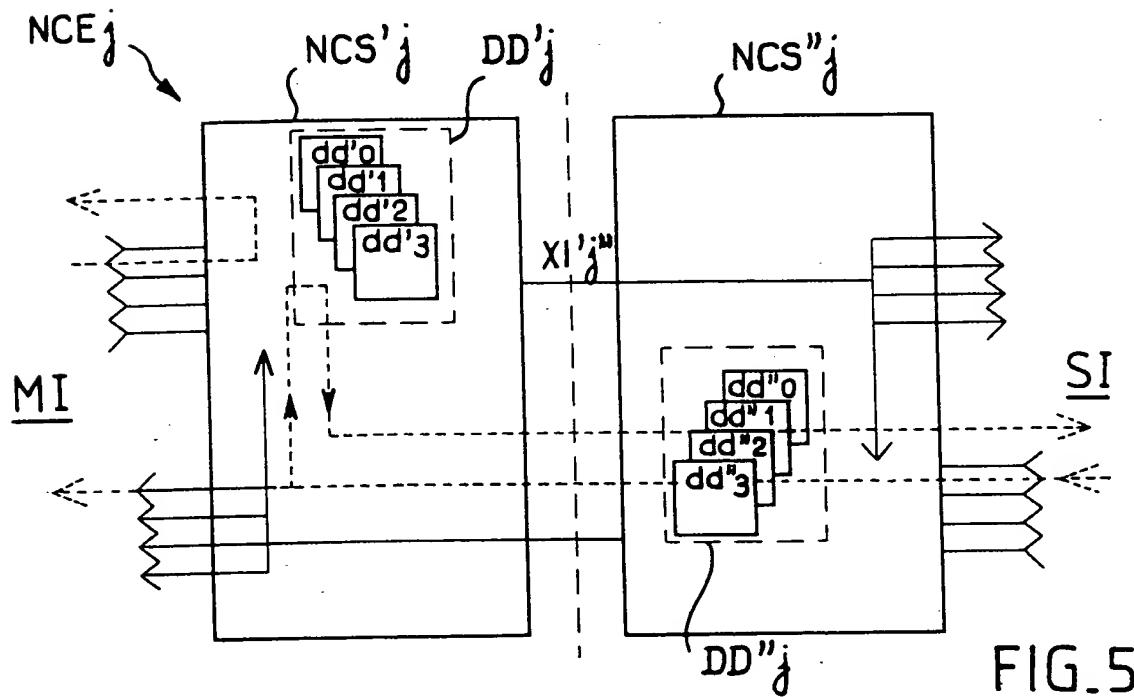
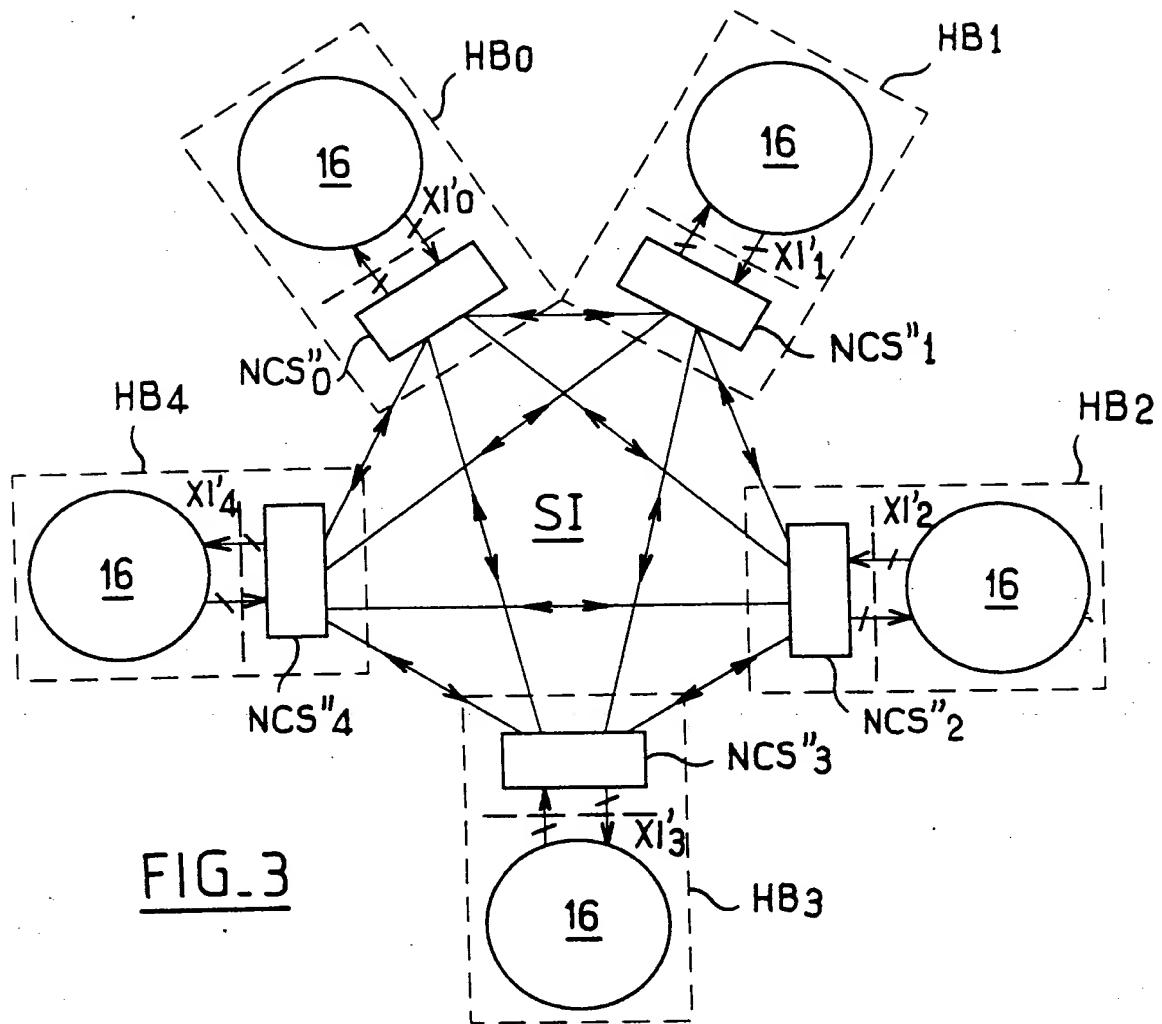
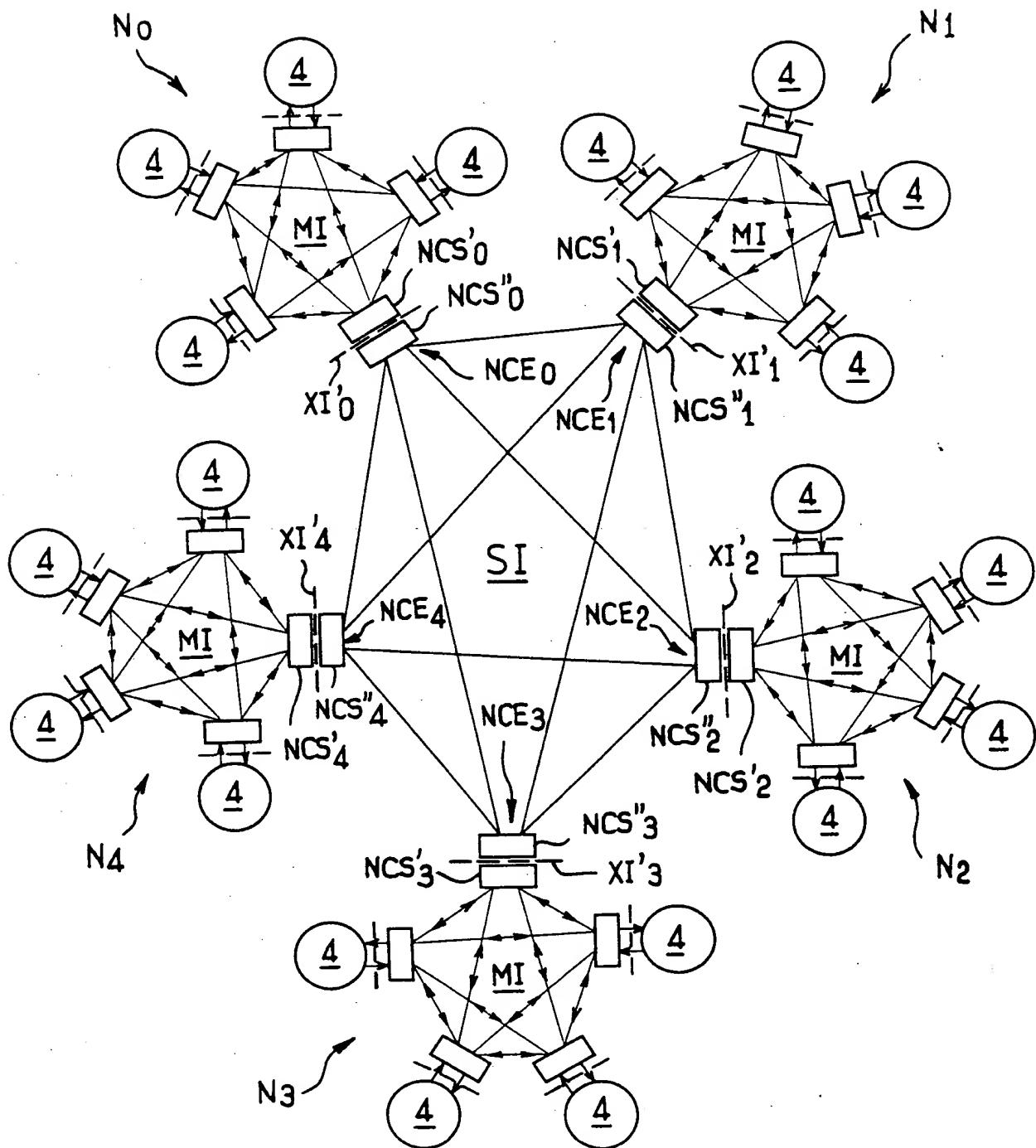


FIG.2

~~2/5~~

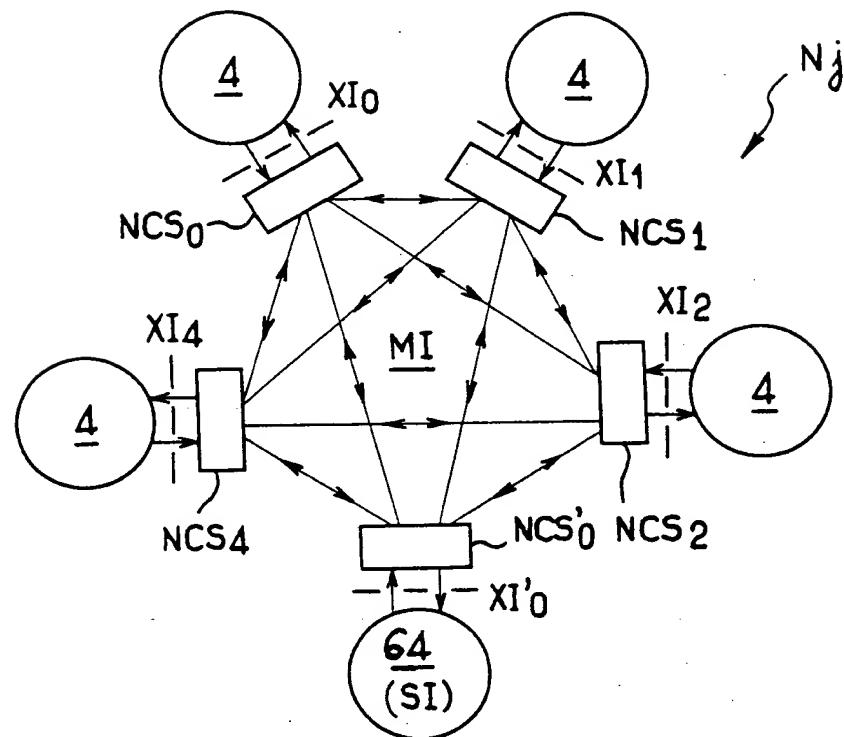


~~3/5~~

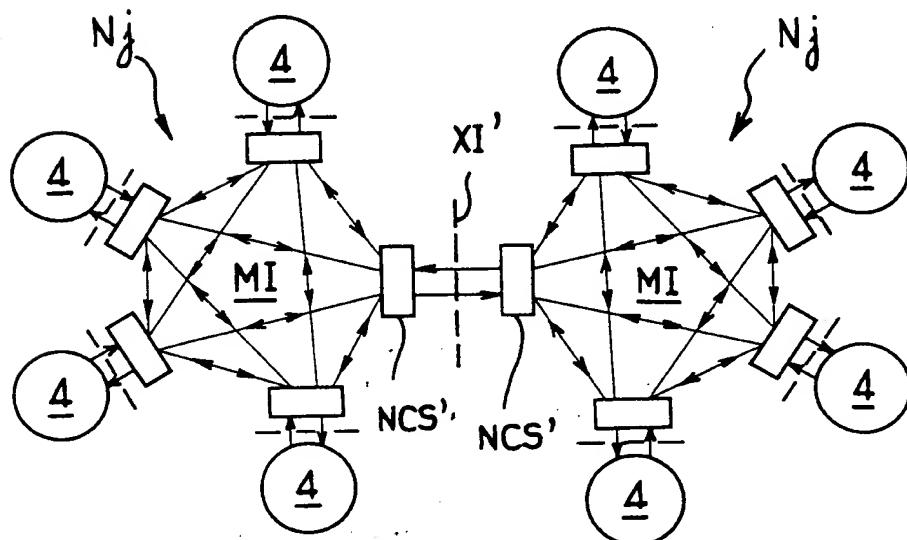


FIG\_4

4 / 5



FIG\_6



FIG\_8

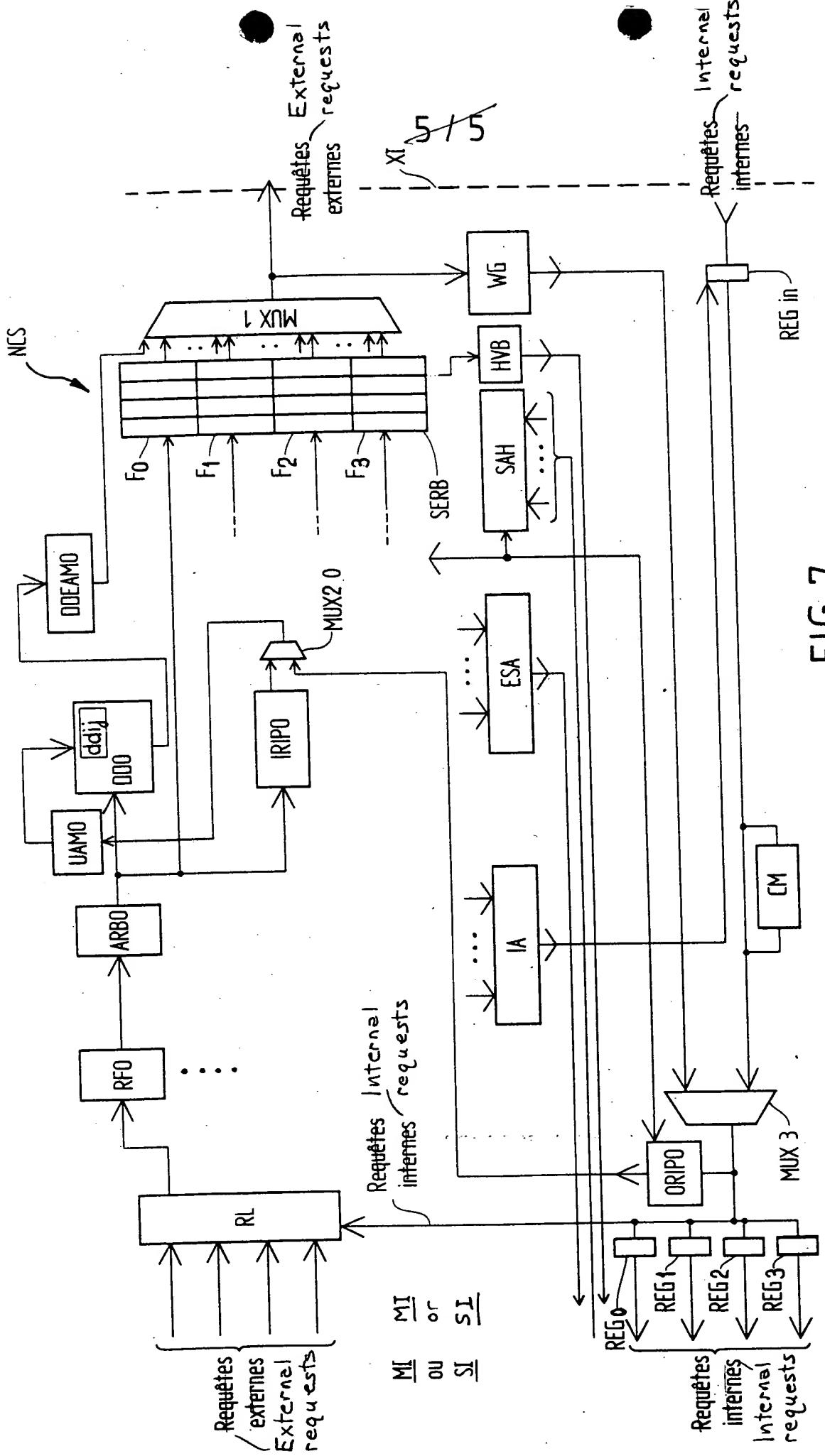


FIG. 7